Utilizing PSCAD in Designing Detection Logic for Ground Fault Overvoltage

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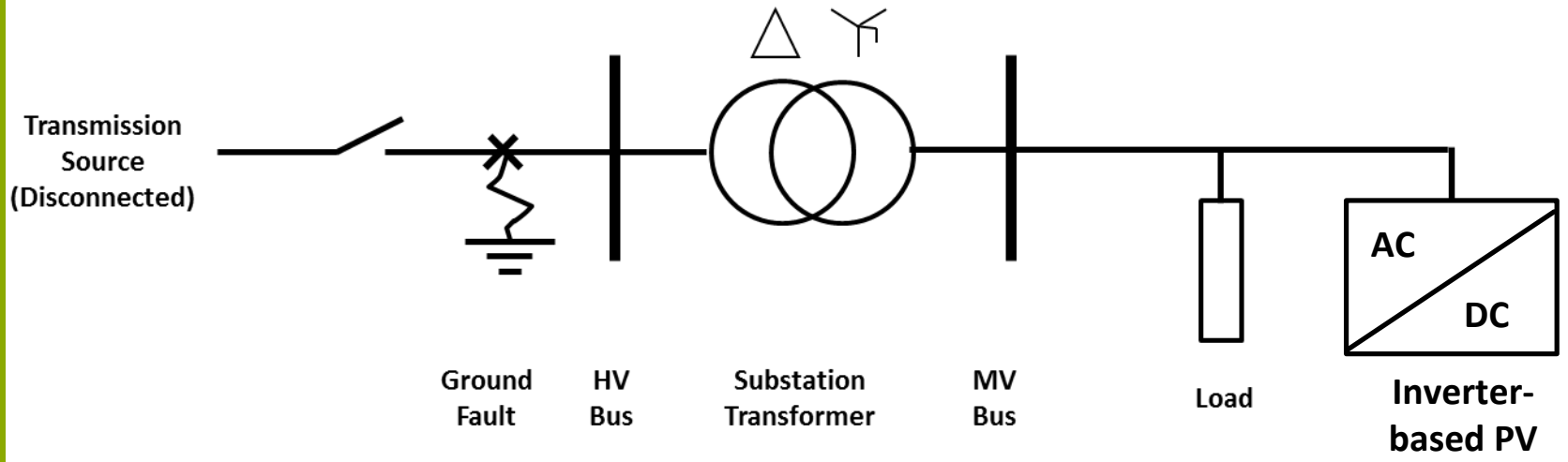
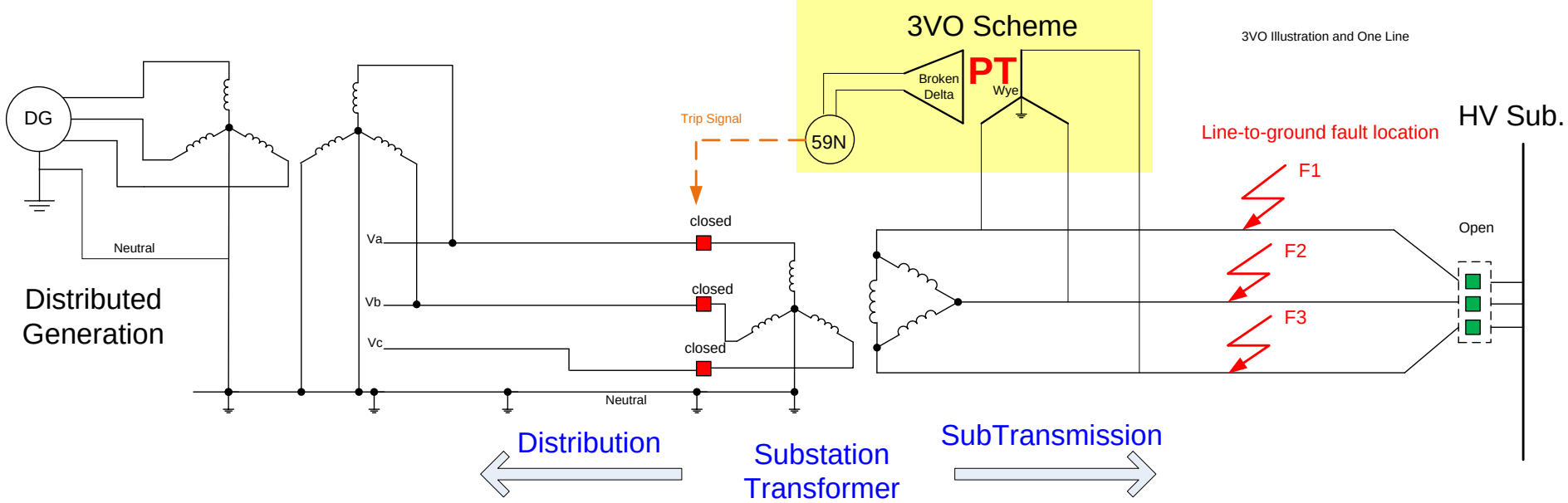
PSCAD User Group Meeting Atlanta, GA.
August 20-21, 2018

Background

- When connecting inverter-based PV generation to the electrical distribution grid, many interconnection challenges exist: islanding, load rejection, reverse power flow, power quality, etc.
- One of the recent issues is GFOV on sub-transmission system caused by PV generation on distribution circuit



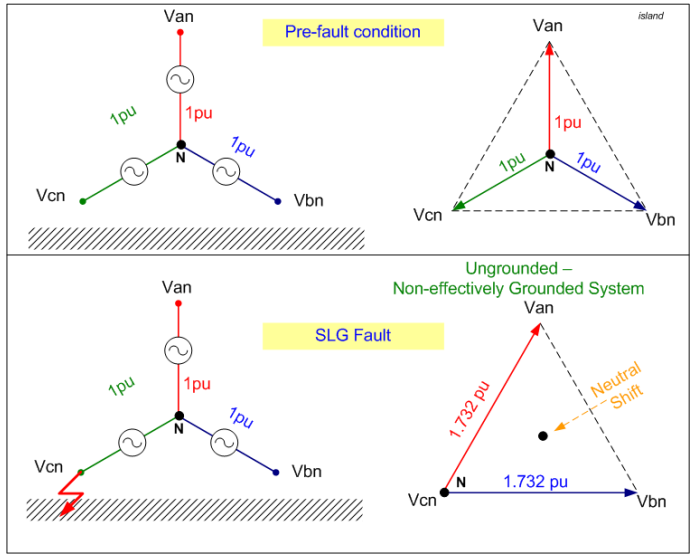


Event sequence

- SLG fault occurs on subtransmission
- Fault detected
- Subtransmission breaker opens islanding the faulted line and distribution feeders with DG
- DGs on the island do not trip fast enough
- Not enough load on the island to depress voltage
- Overvoltage occurs on the subtransmission line

Utilities require 3Vo scheme

- One mitigation measure is to add PTs on the transformer delta (high) side
- The PTs measure the 3Vo voltage to identify an overvoltage
- Relays send signals to trip DG or other breakers to eliminate the overvoltage
- **Expensive ($500K) and 0.5 – 1 year to build**



- Adding PTs to existing substation could be difficult due to the space limitation

Alternative to 3V0 Scheme

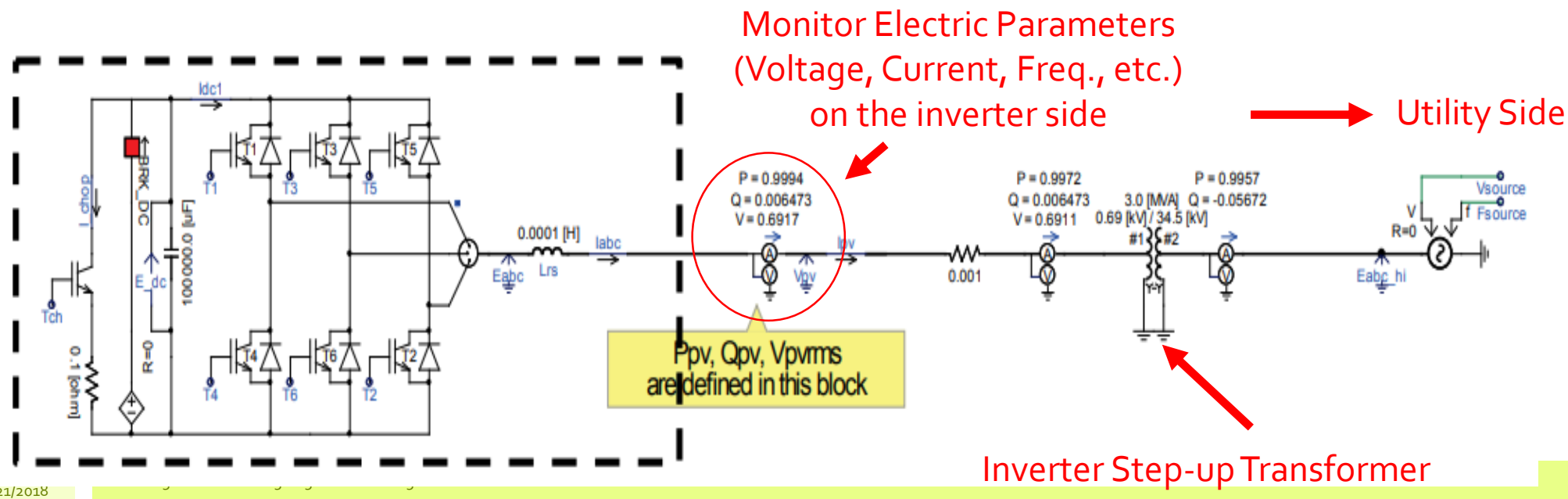
Objectives:

Cost effective

Respond faster

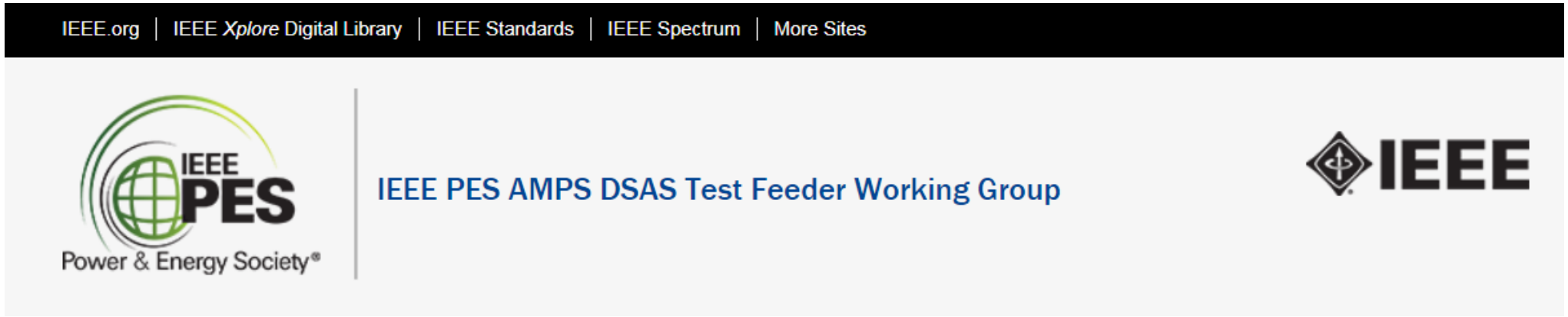
Focus of investigation:

- Detection on the low-voltage side of the substation transformer
- Do not require extensive amounts of additional equipment, material or construction
- Monitor parameters that distinctly identify a potential GFOV condition without being overly subject to over sensitivity (such as nuisance tripping) or under sensitivity (such as failing to detect the onset or presence of GFOV)



Grid / Distribution Feeder Model

- Four test feeders
  - Test Feeder #1: IEEE 4 Node Feeder , modified to 5 nodes to include Substation Transformer
  - Test Feeder #2: 12 km long, 25 kV Radial Feeder
  - Test Feeder #3: IEEE 13 Node Feeder (Short Feeder)
  - Test Feeder #4: IEEE 34 Node Feeder (very Long Feeder, Actual feeder located in Arizona)



Inverter Model

Five different inverter models

1. Inverter model #1: 250 kW, three-phase, potential GFOV issue, “blackbox”
2. Inverter model #2: 250 kW, three-phase, high sensitivity to ground faults , “blackbox”
3. Inverter model #3: 1 MW, three-phase, potential GFOV issue, “blackbox”
4. Inverter model #4: 1 MW, power regulated current source inverter, NREL, “generic”
5. Inverter model #5: 500 kW, power regulated voltage source inverter with MPPT, MHRC, “generic”

Two Commercial Inverters are able to detect the SLG fault and trip very fast (cannot be used to test the NSV logic)

Inverter 1 , 4 and 5 are used in multiple inverter cases

Commercial Inverters UL-1741 Certified with “blackbox” model

Generic Inverter Models with two different control strategies developed by NREL and MHRC

Alternate to 3V0 Scheme (NSV Protection Scheme)

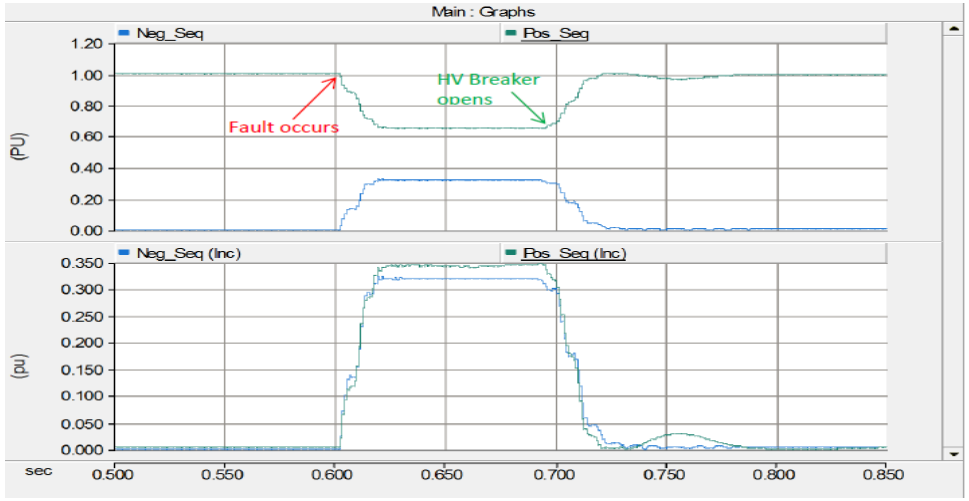
Try these parameters:

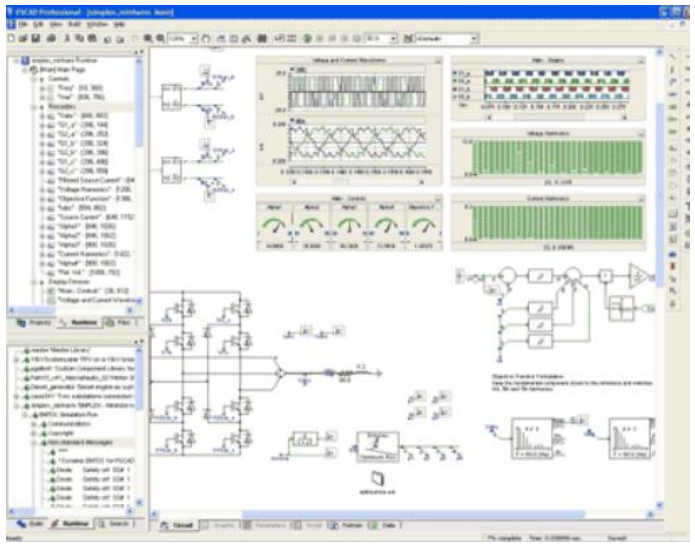
- Voltage imbalance
- Negative sequence current
- Negative sequence directional
- Transient voltage rate of rise
- Many other parameters…

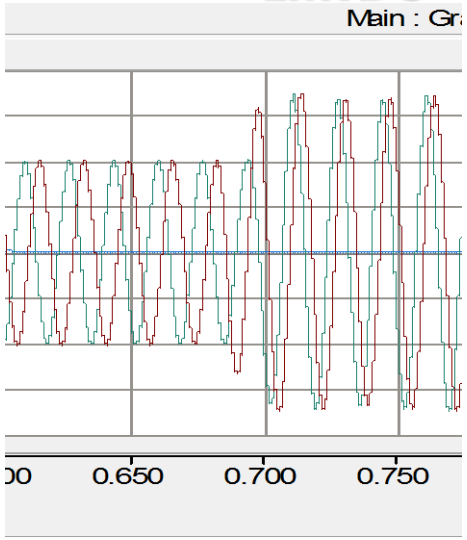
Most effective:

- Negative sequence voltage jump
- Ratio of negative and positive sequence voltages

Pterra modeled and simulated the model utilizing PSCAD EMTC software





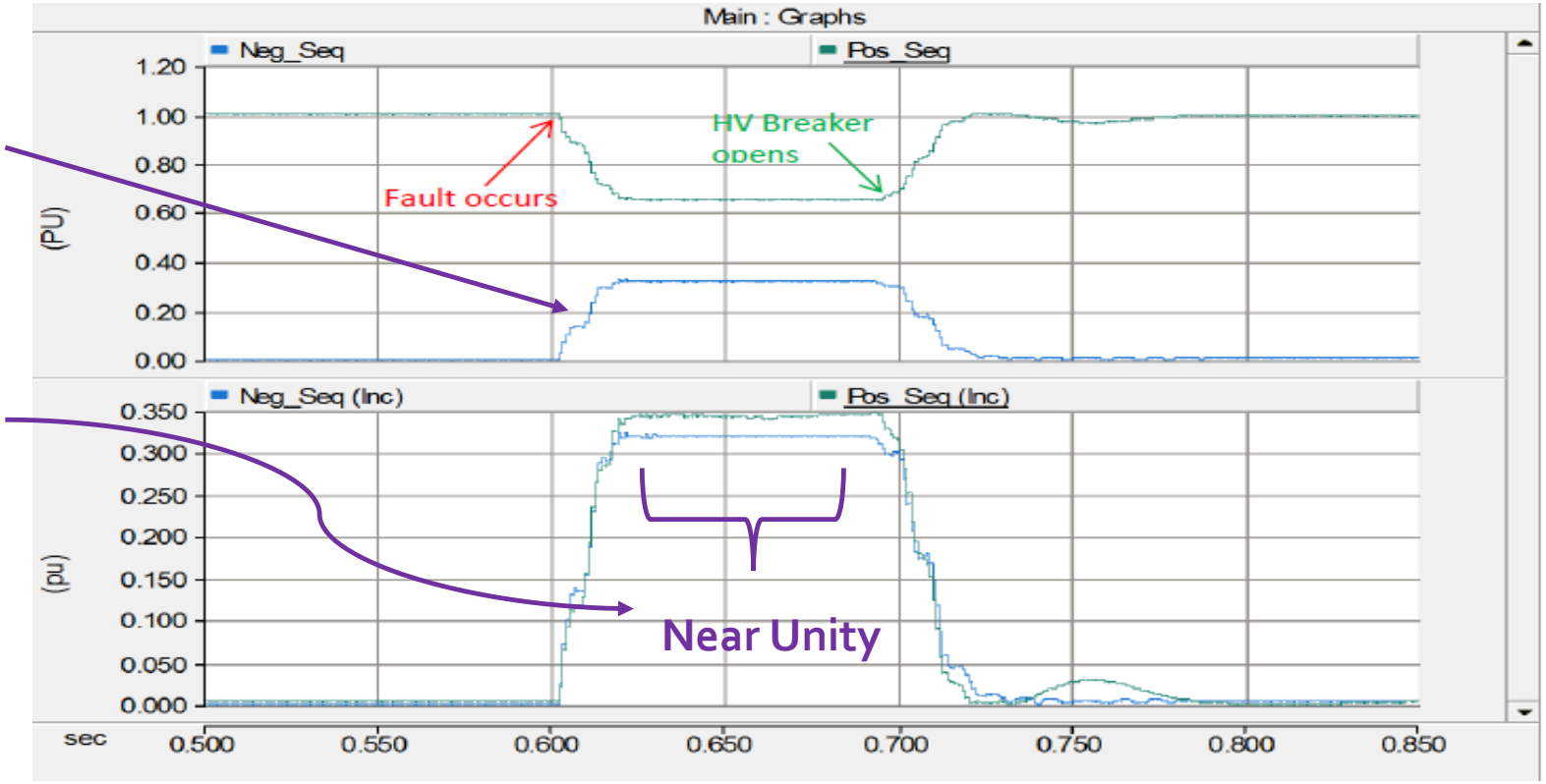


NSV Protection Scheme

SLG fault on transmission monitor signals on the inverters side!

General Logic Discussion:

1. Immediately after the SLG fault is applied, the positive sequence voltage drops while the negative sequence voltage rises rapidly.
2. Shortly after the SLG fault occurs, the ratio of incremental negative sequence voltage to incremental positive sequence voltage is near unity.
3. The ratio remains near unity until the HV breaker opens, when the negative sequence shows a sudden decrease.



NSV Protection Scheme

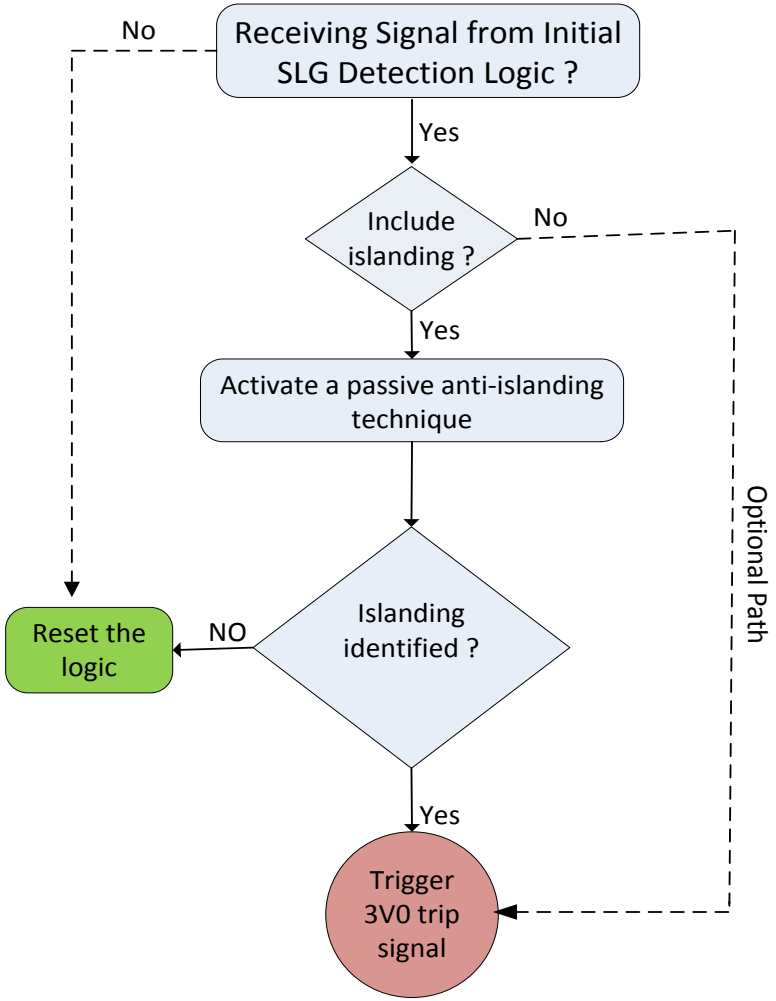
Two Options for completing the scheme after the initial SLG detection logic:

Option 1:

1. Immediately send out trip signal after about 5 cycles (sub-transmission breaker opening time)

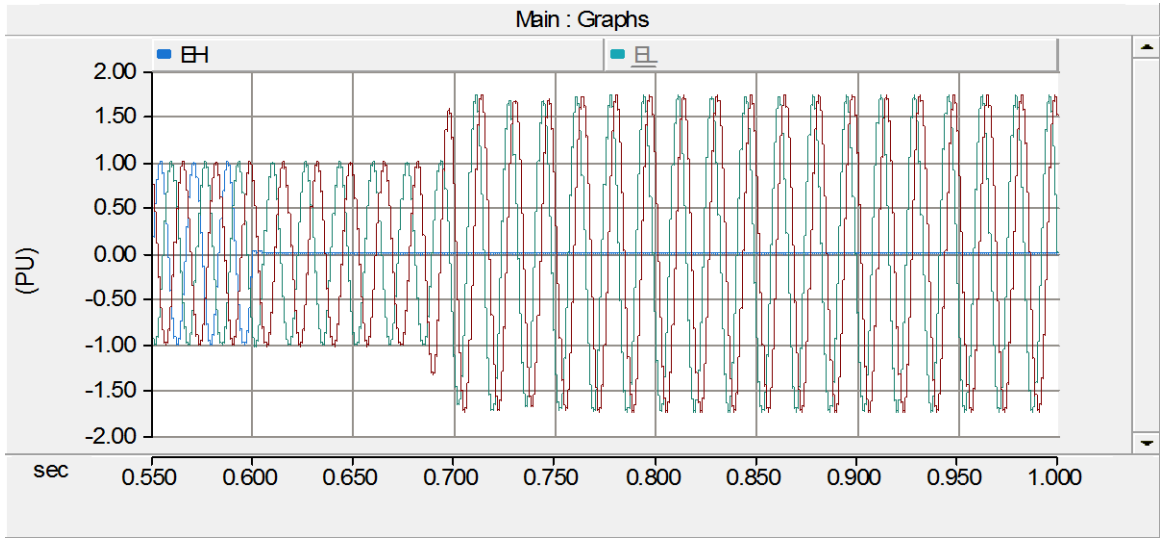
Option 2:

1. Activate islanding detection logic
2. If SLG Fault and Islanding are true, then trip the inverter

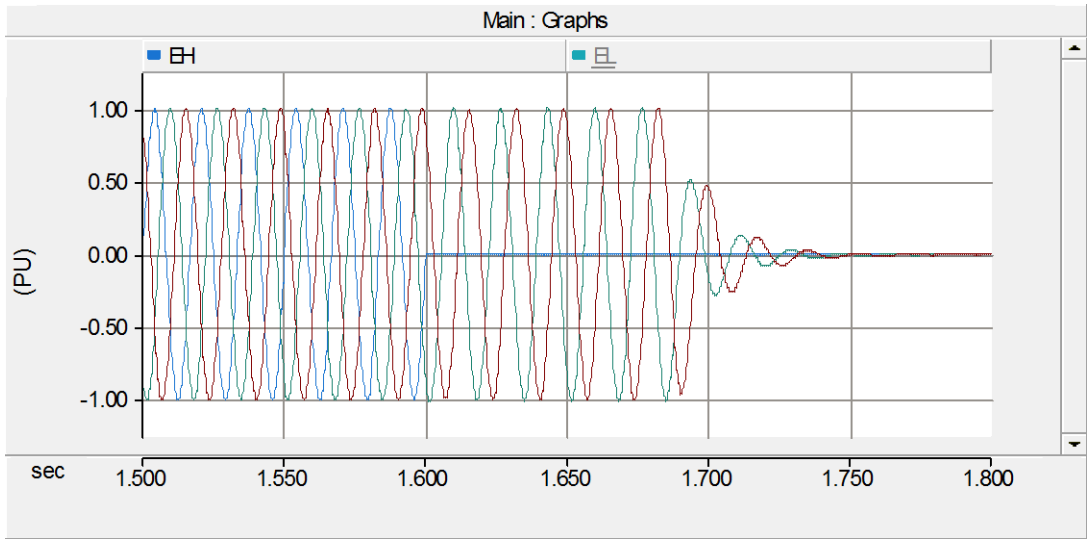


NSV Simulation – One Inverter Case without NSV Scheme

Test Case #4: Voltage at Primary Side of Substation Transformer following SLG Fault – Inverter #1, weak grid



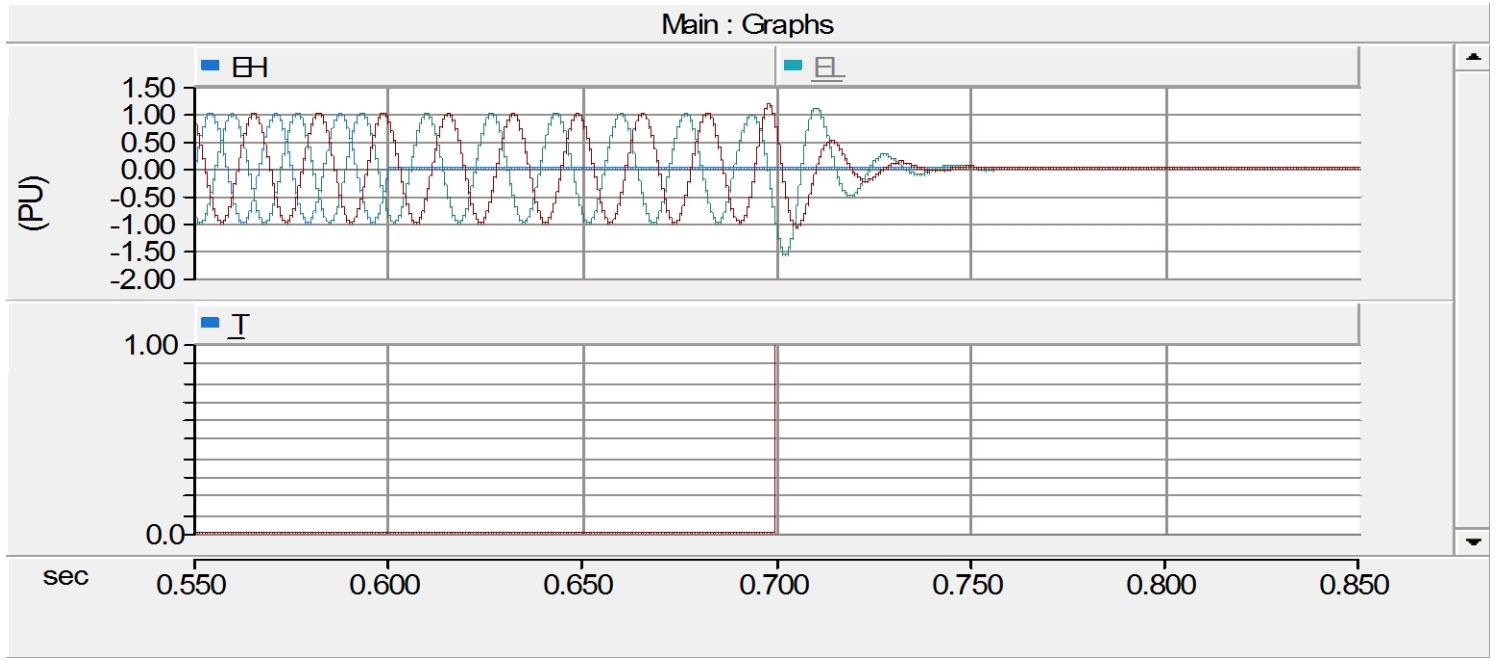
Test Case #8: Voltage at Primary Side of Substation Transformer following SLG Fault – Inverter #3, weak grid



- Inverter#1 is unable to detect the faulted condition and stays online. GFOV is observed on the primary side of the substation transformer (delta side) after the HV breaker opens.
- Inverter #3 is sensitive to the faulted condition. No ground fault overvoltage is observed in test cases with inverter#3

NSV Simulation – One Inverter Case with NSV Scheme

Test Case #4 with NSV Scheme: Voltage at Primary Side of Substation Transformer following SLG Fault – Inverter #1



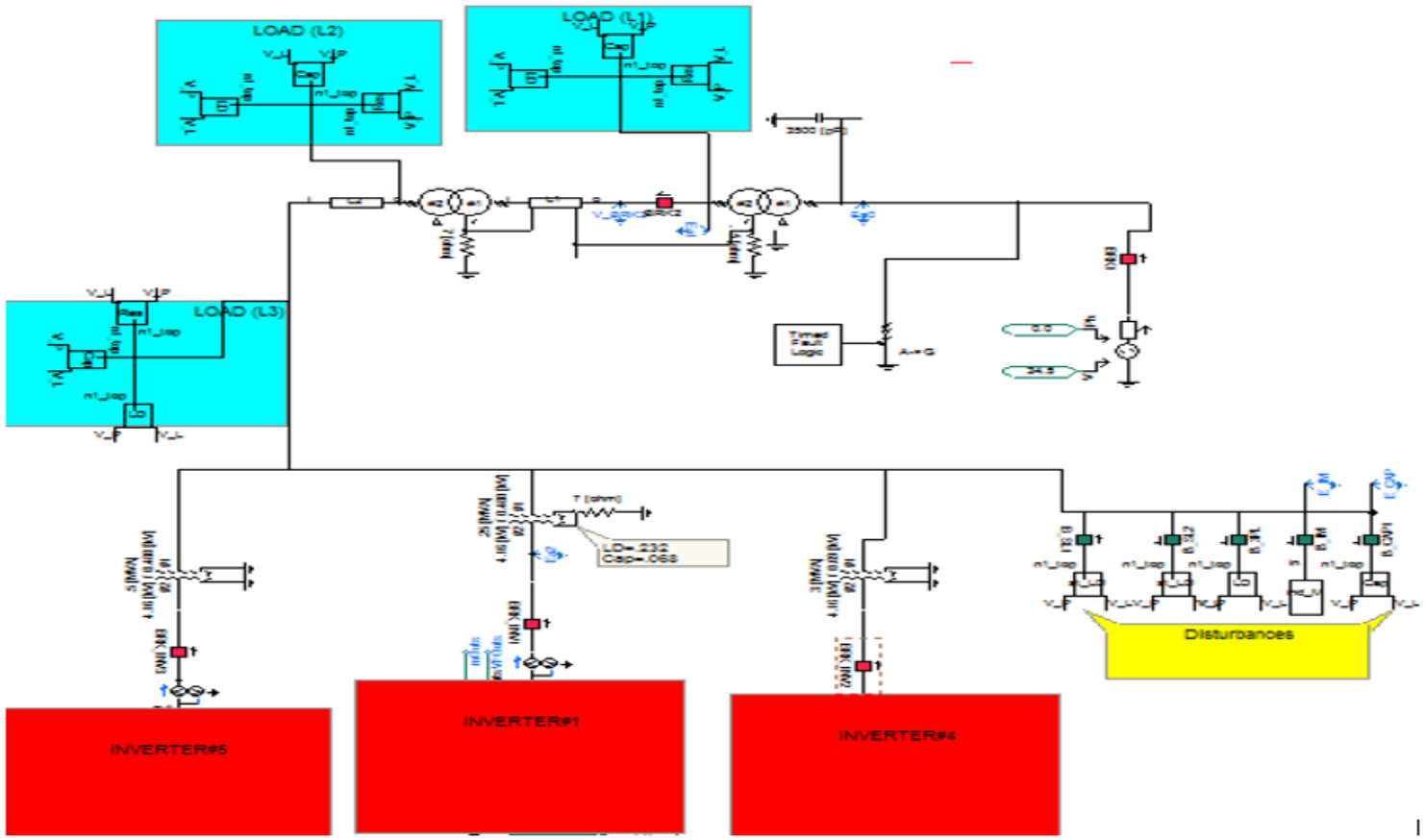
- At 0.6 s, the SLG fault is applied
- At 0.6833 s, the HV breaker opens
- At 0.7 s, the NSV logic issues a trip signal
- By 0.75 s, voltages on the high side are essentially zero

(*) The logic with islanding detection trip inverter within 4 cycles after the breaker open

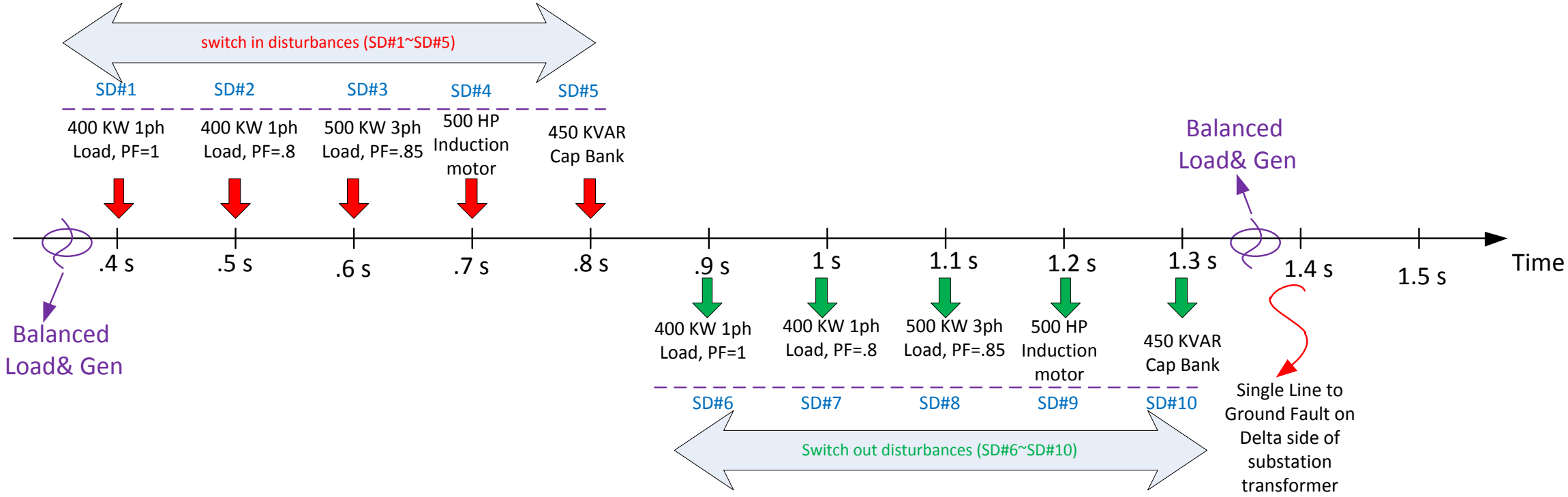
(*) The logic without islanding detection can trip inverter just before breaker opens

NSV Simulation – Multiple Inverters Case

Top View of the PSCAD Model-Test Case#17 showing location of Inverters in Test Feeder #1



NSV Simulation – Additional Switching Disturbances

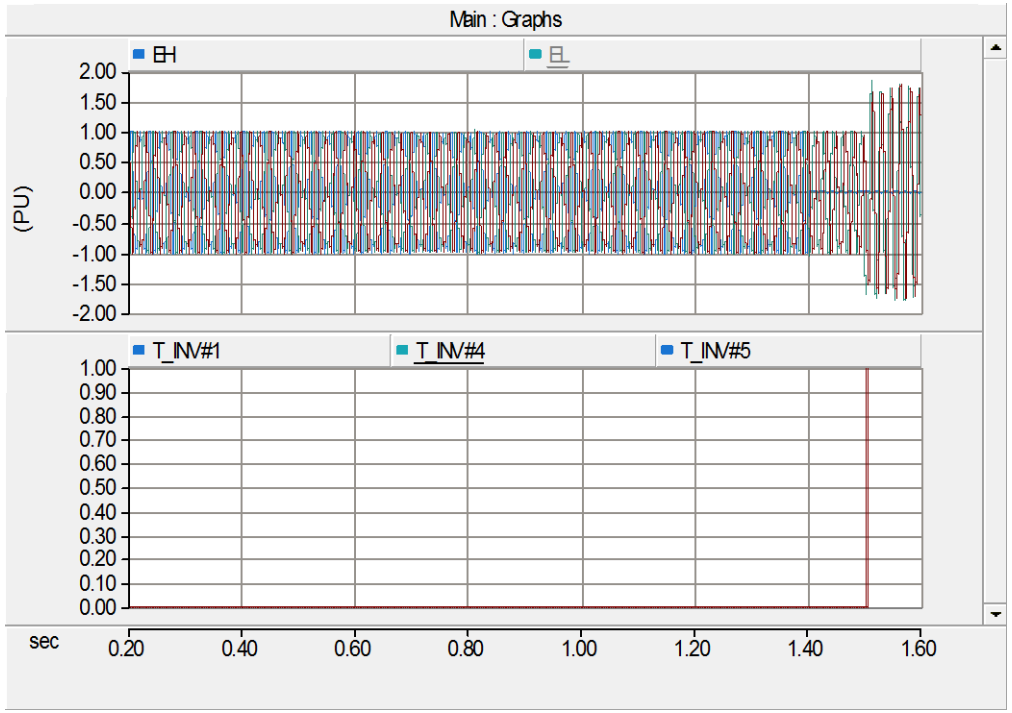


Note:

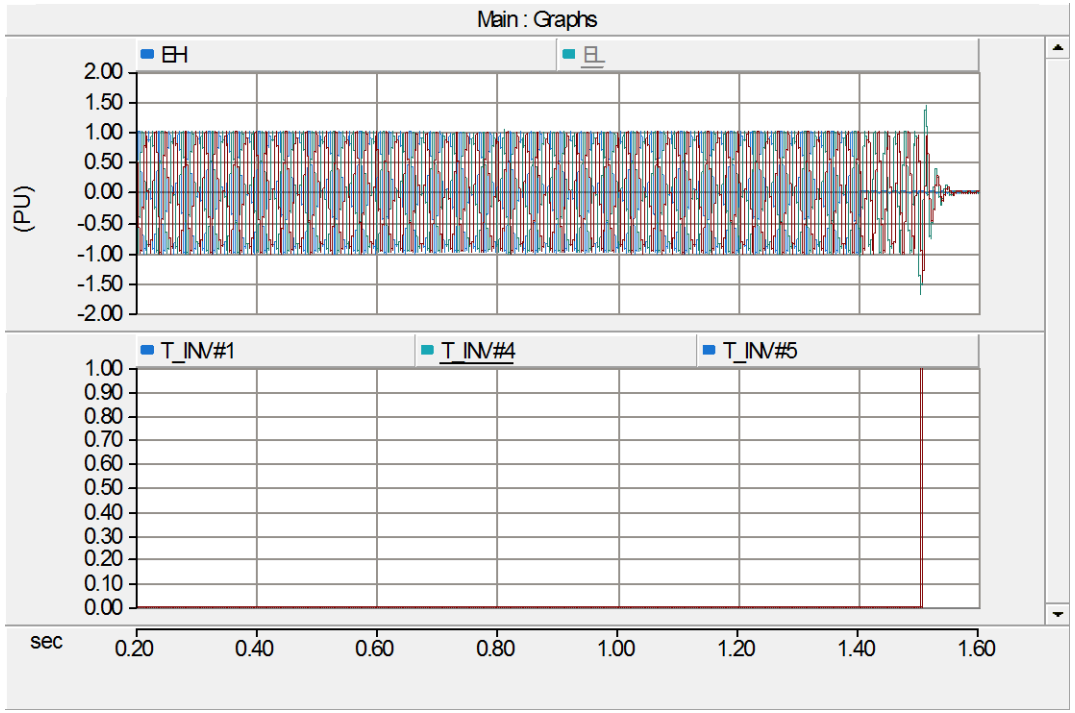
- The distributed loads, L1, L2 and L3, in each test case are tuned such that current passing from the upstream circuit breaker would be close to zero before the occurrence of first disturbance and shortly after the last disturbance.

NSV Simulation

Voltage at Primary Side of Substation Transformer (top) and the Logic Trip Signals (bottom)- Test Case#18



Voltage at Primary Side of Substation Transformer (top) and the Logic Trip Signals (bottom)- Test Case#26



- The NSV is not triggered by the miscellaneous switching events and is able to recognize the potential GFOV and trip the associated PV in a few cycles.

What's Next?

- Testing the logic with Hardware in the loop
- OPAL-RT / RTDS
- Is there a way to convert from PSCAD to Matlab?

Conclusion

- The research findings confirm that the need for the expensive PTs and 0.5-1 year construction time may be avoided with the NSV protection scheme with a detailed design of the NSV implementation at individual PV inverters

- The concept would need to be confirmed with a detailed design of the NSV implementation at individual PV inverters. Testing the scheme with programmed inverters through a hardware-in-the-loop (HIL) simulation is a possible next step to further evaluate the NSV scheme.

- Field tests can be conducted with devices that support the NSV protection scheme to verify that the performance matches the simulations.